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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/539,549	06/16/2005	Petrus Hubertus Magnee	BE02 0044 US1	7976

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EXAMINER	
RAO, G NAGESH	

ART UNIT	PAPER NUMBER
1714	

NOTIFICATION DATE	DELIVERY MODE
05/17/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/539,549	MAGNEE ET AL.	
	Examiner	Art Unit	
	G. NAGESH RAO	1714	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Specification

1) The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and

if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Content of Specification

(a) Title of the Invention: See 37 CFR 1.72(a) and MPEP § 606. The title of the invention should be placed at the top of the first page of the specification unless the title is provided in an application data sheet. The title of the invention should be brief but technically accurate and descriptive, preferably from two to seven words may not contain more than 500 characters.

(b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.

(c) Statement Regarding Federally Sponsored Research and Development: See MPEP § 310.

(d) The Names Of The Parties To A Joint Research Agreement: See 37 CFR 1.71(g).

(e) Incorporation-By-Reference Of Material Submitted On a Compact Disc: The specification is required to include an incorporation-by-reference of electronic documents that are to become part of the permanent United States Patent and Trademark Office records in the file of a patent application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text were permitted as electronic documents on compact discs beginning on September 8, 2000.

(f) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification

definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

(2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

(g) Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

(h) Brief Description of the Several Views of the Drawing(s): See MPEP § 608.01(f). A reference to and brief description of the drawing(s) as set forth in 37 CFR 1.74.

(i) Detailed Description of the Invention: See MPEP § 608.01(g). A description of the preferred embodiment(s) of the invention as required in 37 CFR 1.71. The description should be as short and specific as is necessary to describe the invention adequately and accurately. Where elements or groups of elements, compounds, and processes, which are conventional and generally widely known in the field of the invention described and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail. However, where particularly complicated subject matter is involved or where the elements, compounds, or processes may not be commonly or widely known in the field, the specification should refer to another patent or

readily available publication which adequately describes the subject matter.

(j) Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on separate sheet or electronic page (37 CFR 1.52(b)(3)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).

(k) Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

(l) Sequence Listing. See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431. The requirement for a sequence listing applies to all sequences disclosed in a given application, whether the sequences are claimed or not. See MPEP § 2421.02.

Examiner notes the format of the specification does not properly follow the guidelines set above and is objecting to the current format put forth by the applicant. Examiner has noted that the application claims PCT 371 and Foreign priority for the claimed invention. Examiner reminds applicant to include in amended specification:

(b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2) Claims 1-5 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Wild (US Patent No. 5,310,698).

Wild 698 pertains to the process for producing an Arsenic doped smooth polycrystalline silicon layer for very large scale integrated circuits. Wild 698 teaches the method of making such a semiconductor device typically used for DRAM as can be seen in Figure 1, a monocrystalline Silicon substrate with an Arsenic layered ontop followed by an amorphous polysilicon that reacts to transform into a polycrystalling structure followed by a layered capping of SiO_2 layer ontop, during which time the substrate is heat treated, deposited with an arsenic gaseous compound as well simultaneously with a gaseous silicon compound, by which the temperature range for fabrication falls within the

prescribed 400-600^{0}C range and a pressure of 12-20 Pa (When converted to unit of mTorr is well below the 500 mTorr limit) which fall within the claimed limitation by applicant (See Figure 2, Abstract, Cols 3-6 Lines 1-68).

3) Claims 1-3, 5, and 7-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamasaki (US Patent No. 5,250,448).

Hamasaki 448 pertains to the process for producing an Arsenic doped smooth polycrystalline silicon layer for very large scale integrated circuits. Hamasaki 448 teaches the method of making such a semiconductor device typically used for DRAM as can be seen in Figures 1A-1M, a monocrystalline Silicon substrate with an Arsenic layered ontop followed by an amorphous polysilicon that reacts to transform into a polycrystalling structure followed by a layered capping of SiO_2 layer ontop, during which time the substrate is heat treated, deposited with an arsenic gaseous compound as well simultaneously with a gaseous silicon compound, by which the capping layer will be a SiGe layer, and contacts of a single crystal layer through the window (See Figures 1A-1M, Cols 3-4 Lines 1-68).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4) Claims 6-7, and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wild (US Patent No. 5,310,698) in view of Todd (US Patent No. 6,821,825).

From the aforementioned rejection pertaining to Wild 698, it is taught to fabricate a semiconductor device reading on applicant's claimed invention. However Wild 698 fails to mention the fabrication of said device with a SiGe capping layer over said device.

In analogous art pertaining to semiconductor fabrication, Todd 825 teaches a similar device with a SiGe capping layer along with a small percentage of carbon additive to the mix (See Abstract, Figs 1-2, Cols 9-10 Lines 1-68).

It would be obvious to one having ordinary skill in the art at the time of the present invention and based on motivations suggested by Todd 825 to incorporate the SiGe with carbon additive layer in order to "...the invention relates to making these materials with greater thickness and compositional uniformity in chemical vapor deposition systems.", as well "As the dimensions of microelectronic devices become smaller, the importance of the physical and chemical properties of the materials used in their manufacture becomes more important. This is particularly true for those advanced materials that can be integrated into existing generations of devices using already-proven manufacturing tools. For example, it would be desirable to incorporate epitaxial Si.sub.1-x Ge.sub.x and Si.sub.1-x-y Ge.sub.x C.sub.y alloys into Bipolar and BiCMOS device manufacturing processes. These advanced alloy materials have utility as base layers in heterojunction bipolar transistors (HBT), resistors in BiCMOS devices and as gate electrodes in CMOS devices and various other integrated electronic devices. Conventional processes for the deposition of single crystal, amorphous and/or polycrystalline silicon, silicon germanium (SiGe) and silicon germanium carbon (SiGeC) alloys are typically

performed using batch thermal processes (either low pressure (LP) or ultra-high vacuum (UHV) conditions) or single wafer processes. Single wafer processes are becoming increasingly significant..." (See Col 1 Lines 21-45).

5) Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamasaki (US Patent No. 5,250,448) in view of Todd (US Patent No. 6,821,825).

From the aforementioned rejection pertaining to Hamasaki 448, it is taught to fabricate a semiconductor device reading on applicant's claimed invention. However Hamasaki 448 fails to mention the fabrication of said device with a SiGe capping layer over said device containing a carbon additive nor the appropriate temperature and pressure processing range for fabricating these devices.

In analogous art pertaining to semiconductor fabrication, Todd 825 teaches a similar device with a SiGe capping layer along with a small percentage of carbon additive to the mix as well the appropriate temperature and pressure ranges (See Abstract, Figs 1-2, Cols 9-10 Lines 1-68).

It would be obvious to one having ordinary skill in the art at the time of the present invention and based on motivations suggested by Todd 825 to incorporate

the processing conditions and SiGe with carbon additive layer in order to "…the invention relates to making these materials with greater thickness and compositional uniformity in chemical vapor deposition systems.", as well "As the dimensions of microelectronic devices become smaller, the importance of the physical and chemical properties of the materials used in their manufacture becomes more important. This is particularly true for those advanced materials that can be integrated into existing generations of devices using already-proven manufacturing tools. For example, it would be desirable to incorporate epitaxial Si.sub.1-x Ge.sub.x and Si.sub.1-x-y Ge.sub.x C.sub.y alloys into Bipolar and BiCMOS device manufacturing processes. These advanced alloy materials have utility as base layers in heterojunction bipolar transistors (HBT), resistors in BiCMOS devices and as gate electrodes in CMOS devices and various other integrated electronic devices. Conventional processes for the deposition of single crystal, amorphous and/or polycrystalline silicon, silicon germanium (SiGe) and silicon germanium carbon (SiGeC) alloys are typically performed using batch thermal processes (either low pressure (LP) or ultra-high vacuum (UHV) conditions) or single wafer processes. Single wafer processes are becoming increasingly significant…" (See Col 1 Lines 21-45, Cols 3-7 Lines 1-68).

Response to Arguments

6) Applicant's arguments filed 2/25/08 have been fully considered but they are not persuasive. Upon review of applicant's remarks and the filed claims in contrast to the prior art, it is the examiner's position that the references applied are still applicable at this time.

With respect to the specification, examiner understands that it is the applicant's wish whether to comply with the suggested specification format desired by the agency. However the way the specification is presented causes concern for what section attributes to what corresponding written paragraphs. Therefore objection will be maintained at this time.

With respect to the 102(b) rejection of claims 1-5 under Wild 698, examiner points to Col 3 Lines 38-40 which discloses teaching of an arsenic layer. In addition to Figure 2 which does depict an arsenic layer that is formed on the monocrystalline silicon layer. Furthermore the arsenic layer is not formed on a region of silicon oxide (also see Col 4 Lines 4-24), if anything an amorphous polysilicon layer is formed on the arsenic layer (see Figure 2). There is nothing in the claim that indicates the monocrystalline silicon and silicon oxide having to be situated next to each other laterally, as applicant's are appearing to denote in the argument.

With respect to the 102(b) rejection of claims 1-3, 5, and 7-8, Hamasaki 448 does appear to indicate an arsenic type layer which still constitutes as a layer formed in a monocrystalline layer (there is no specified thickness denoted in the claimed invention) (Col 3 Lines 14-25). There is nothing in the claim that indicates the monocrystalline silicon and silicon oxide having to be situated next to each other laterally, as applicant's are appearing to denote in the argument.

With respect to the 103(a) rejection, the arguments are based on the premise that Wild and Hamasaki respectively failed to teach the claimed invention, which examiner pointed out contrarily not being the case. Therefore at this time, those arguments are seen as moot.

Conclusion

7) Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened

statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to G. NAGESH RAO whose telephone number is (571)272-2946. The examiner can normally be reached on 8:30AM-5PM (INDEPENDENT FLEX SCHEDULE).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael KORNAKOV can be reached on (571)272-1303. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/G. Nagesh Rao/
Patent Examiner
AU 1714